

NCCT

PROMISE FOR THE BEST PROJECTS

VLSI PROJECTS

IEEE PROJECTS in various Domains
Latest Projects, 2009 - 2010

#109, 2nd Floor, Bombay Flats, Nungambakkam High Road
Nungambakkam High Road, Chennai – 600034

Above IOB, Next to ICICI

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EMBEDDED SYSTEM PROJECTS
Microcontrollers | VLSI | DSP | Matlab | Robotics

VLSI PROJECTS

- An Area-Efficient Universal Cryptography Processor for Smart Cards – 2009
- The CSI Multimedia Architecture – 2009
- FPGA Based Power Efficient Channelizer for Software Defined Radio – 2009
- Improvement of the Orthogonal Code Convolution Capabilities using FPGA Implementation – 2009
- A VHDL Model of a IEEE1451.2 Smart Sensor: Characterization and Applications – 2008
- Fuzzy based PID Controller using VHDL/VERILOG for Transportation Application – 2008
- Implementation of IEEE 802.11 a WLAN baseband Processor – 2008
- A Lossless Data Compression and Decompression Algorithm and its Hardware Architecture – 2008
- A Verilog Implementation of UART Design with Bist Capability – 2008
- A Robust Uart Architecture based on Recursive Running Sum Filter for Better Noise Performance – 2008
- FPGA Implementation of USB Transceiver Macrocell Interface with Usb2.0 Specifications

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- **A VLSI Architecture for Visible Watermarking In A Secure Still Digital Camera (S2dc) Design (Corrected)**
- **A Low-Power Multiplier with the Spurious Power Suppression Technique**
- **Design of Reconfigurable Coprocessor for Communication Systems**
- **Block-Based Multiperiod Dynamic Memory Design for Low Data-Retention Power**
- **A Symbol-Rate Timing Synchronization Method for Low Power Wireless OFDM Systems**
- **On the Design of a Multi-Mode Receive Digital-Front-End for Cellular Terminal RFICS**
- **Design Exploration of a Spurious Power Suppression Technique (SPST) and its Applications**
- **Implementation of a Multi-Channel UART Controller based on FIFO Technique and FPGA**
- **Compliant Digital Baseband Transmitter on a Digital Signal Processor**
- **An FPGA-Based Architecture for Real Time Image Feature Extraction**
- **FPGA based Generation of High Frequency Carrier for Pulse Compression Using Cordic Algorithm**
- **VLSI Architecture and FPGA Prototyping of a Digital Camera for Image Security and Authentication**

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- VLSI Design & Implementation of Cellphone Controller using VHDL
- VLSI Design & Implementation of Code Converters using VHDL
- VLSI Design & Implementation of Electronic Automation using VHDL
- VLSI Design & Implementation of Arithmetic Logic Unit using VHDL
- VLSI Design & Implementation of Encryption & Decryption using VHDL
- VLSI Design & Implementation of Bus Arbiter using VHDL
- VLSI Design & Implementation of Data Routing Multiplexer using VHDL
- VLSI Design & Implementation of DMA using VHDL
- VLSI Design & Implementation of Water Pump Controller using VHDL
- VLSI Design & Implementation of Associate Memory using VHDL
- VLSI Design & Implementation of I2c Controller Core
- VLSI Design & Implementation of Stepper Motor Controller
- VLSI Design & Implementation of Basic RSA Encryption Engine
- VLSI Design & Implementation of Basic Des Crypto Core
- VLSI Design & Implementation of Fuzzy Controller Design

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- **Optimized Software Implementation of a Full-Rate IEEE 802.11a**
- **VLSI Design & Implementation of Fir & Lir Designing**
- **VLSI Design & Implementation of Home Appliances Control Designing**
- **VLSI Design & Implementation of Electronic Voting Machine**
- **VLSI Design & Implementation of Security System**
- **VLSI Design & Implementation of Robot Controller**
- **VLSI Design & Implementation of Solar Panel Control**
- **VLSI Based Temperature Controller Implementation**
- **VLSI Based Motor Speed Controller**
- **Designing of Risc Controller using Verilog Hdl**
- **Designing of I2c Master Core / Spi Master Core using Verilog Hdl**
- **Designing of Pc Printer Port / Serial Port using Verilog Hdl**
- **Designing of Programmable Peripheral Interface (Ppi) using Verilog Hdl**
- **Designing of Programmable Timer Interface (Pti) using Verilog Hdl**
- **Designing of Universal Sync / Async Receiver and Transmitter (Usart)**
- **Design of Industrial PLC**
- **Design of Industrial Robot**

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- Design and Implementation of Elevator Controller
- Design and Implementation of Traffic Light Controller
- Implementation of Data Link Layer Receiver in PCI Express
- Implementation of Data Link Layer Transmitter in PCI Express
- Matrix Multiplication Synthesis
- Implementation of a Multi-Coder Processor for the WTLS with High Compression Ratio
- VHDL Implementation of Cordic Algorithm for Wireless LAN
- Design and Simulation of Synchronization Unit for Wcdma Uplink Receiver
- Design of a Simulator Tool for a Channel with Rayleigh Fading and Awgn Communication
- Emotion Recognition using Facial Expressions
- Design and Implementation of Arithmetic Logic Unit using VHDL
- VLSI Design and Implementation of Associate Memory using VHDL
- VLSI Design and Implementation of Encoder & Decoder using VHDL
- VLSI Design and Implementation of Data Routing Multiplexer using VHDL
- VLSI Design and Implementation of Bus Arbiter using VHDL
- VLSI Design and Implementation of Code Convertors using VHDL

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- VLSI Design & Implementation of Electronic Automation using VHDL
- VLSI Design and Implementation of Encryption & Decryption using VHDL
- VLSI Design and Implementation of Water Pump Controller using VHDL
- VLSI Design and Implementation of Cellphone Controller using VHDL
- A Fast Hardware Approach for Approximate, Efficient Logarithm and Antilogarithm Computations - 2009
- VLSI Design of Diminished-One Modulo $2n + 1$ Adder using Circular Carry Selection - 2009
- The Design and FPGA Implementation of $Gf(2^{128})$ Multiplier for Ghash - 2009
- Bz-Fad: A Low-Power Low-Area Multiplier Based On Shift-and-Add Architecture - 2009
- Novel Area-Efficient FPGA Architectures for Fir Filtering with Symmetric Signal Extension - 2009
- Spread Spectrum Image Watermarking with Digital Design - 2009
- A Generalization of a Fast RNS Conversion for a New 4-Modulus Base - 2009
- Left to Right Serial Multiplier for Large Numbers on FPGA - 2009
- A Compact AES Encryption Core on Xilinx FPGA - 2009

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- **A Fast VLSI Design of Sms4 Cipher Based On Twisted BDD S-Box Architecture - 2009**
- **An improved RC6 algorithm with the same structure of encryption and decryption - 2009**
- **A Novel Multiplexer Based Truncated Array Multiplier - 2009**
- **A New Low Power Test Pattern Generator using A Variable-Length Ring Counter - 2009**
- **Power optimization of linear feedback shift Register (LFSR) for low power BIST - 2009**
- **Deviation-Based LFSR Reseeding for Test-Data Compression - 2009**
- **Fault Secure Encoder and Decoder for Nano-memory Applications - 2009**
- **Hardware Algorithm for Variable Precision Multiplication on FPGA - 2009**
- **Superscalar Power Efficient Fast Fourier Transform FFT Architecture - 2009**
- **A New High-Speed Architecture for Reed-Solomon Decoder - 2009**
- **Low-Power Leading-Zero Counting and Anticipation Logic for High-Speed Floating Point Unit - 2009**
- **Cost-Efficient SHA Hardware Accelerators - 2009**
- **A Framework for Correction of Multi-Bit Soft Errors in L2 Caches based on Redundancy - 2009**

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- **Soft-Error Tolerance and Mitigation in Asynchronous Burst-Mode Circuits - 2009**
- **Tag Overflow Buffering: Reducing Total Memory Energy by Reduced-Tag Matching - 2009**
- **On the Exploitation of Narrow-Width Values for Improving Register File Reliability - 2009**
- **Behavioral Synthesis of Asynchronous Circuits using Syntax Directed Translation as Backend - 2009**
- **Fault Secure Encoder and Decoder for Nano-Memory Applications - 2009**
- **Novel Area-Efficient FPGA Architectures for Fir Filtering With Symmetric Signal - 2009extension**
- **Custom Floating-Point Unit Generation for Embedded Systems - 2009**
- **Design and Synthesis of Programmable Logic Block with Mixed Lut and Macrogate - 2009**
- **Improving Error Tolerance for Multithreaded Register Files - 2008**
- **Area-Efficient Arithmetic Expression Evaluation using Deeply Pipelined Floating Point Cores Using VHDL - 2008**
- **Design Of Reversible Finite Field Arithmetic Circuits with Error Detection – 2008**
- **BZ-Fad: A Low-Power Low-Area Multiplier Based on Shift-and-Add Architecture - 2009**

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- **The Arise Approach for Extending Embedded Processors with Arbitrary Hardware Accelerators - 2009**
- **Variation-Aware Low-Power Synthesis Methodology for Fixed-Point Fir Filters - 2009**
- **Low Power Design of Precomputation-Based Content-Addressable Memory - 2008**
- **L-Cbf: A Low-Power, Fast Counting Bloom Filter Architecture using VHDL - 2008**
- **Low-Power Leading-Zero Counting and Anticipation Logic for High-Speed Floating Point Units – 2008**
- **Low Power Hardware Architecture for Vbsme using Pixel Truncation - 2009**
- **Asynchronous Protocol Converters for Two-Phase Delay-Insensitive Global Communication - 2009**
- **FPGA Implementation(S) of a Scalable Encryption Algorithm - 2008**
- **Design Of Advanced Encryption Standard Using VHDL - 2008**
- **Bit-Swapping LFSR and Scan-Chain Ordering: A Novel Technique for Peak- and Average-Power Reduction In Scan-Based BIST - 2009**
- **Low-Power Scan Testing for Test Data Compression Using A Routing-Driven Scan Architecture - 2009**
- **Enhancement Of Fault Injection Techniques Based On The Modification Of VHDL Code – 2008**

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- **A Full-Adder-Based Methodology for the Design of Scaling Operation In Residue Number System - 2008**
- **FPGA Implementation of Low Power Parallel Multiplier - 2008**
- **Designing Efficient Online Testable Reversible Adders with New Reversible Gate – 2008**
- **Cost-Efficient SHA Hardware Accelerators - 2008**
- **System Architecture and Implementation of MIMO Sphere Decoders On FPGA – 2008**
- **Design of Gps-Gsm Mobile Navigator**
- **VLSI Design of Des(Data Encryption Standard) Algorithm**
- **Implementation Five - Stage Pipelined RISC Processor for Parallel Processing**
- **Design of MPLS Router and Optimization of MPLS Path Restoration Technique using VLSI**
- **Implementation Huffman Coding For Bit Stream Compression In Mpeg - 2**
- **Implementation of Hash Algorithm Used for Cryptography And Security**
- **Implementation of Content Addressable Memory for Atm Applications**
- **Implementation of Scramblers and Descramblers in Fiber Optic Communication Systems – Sonet and Otn**
- **Implementation of Matched Filters Frequency Spectrum in Code Division Multiple Access (Cdma) System and its Implementation**

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- **VLSI Design Of Two Wire Serial EEPROM for Embedded Microcontrollers Specification**
- **High Definition (Hd) Tv Data Encoding and Decoding using Reed Solomon Code**

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